REMARKS

Claims 1-24 are pending. Claims 1, 10, 13, and 18-24 have been amended. In view of the following, all of the claims are in condition for allowance. If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner schedule a teleconference with the Applicant's attorney to further the prosecution of the application.

Rejection of claims 1-8, and 10-24 under §102(b) as being anticipated by Kadowaki et al. (US 5,726,779)

Claim 1

Claim 1, as amended, recites a digitizer operable to receive a serial analog color signal having a predetermined sequence of color components wherein each color component represents a row of pixels of a single color, the digitizer having a plurality of channels each operable to receive the serial analog color signal and to process a respective color component.

For example, referring, *e.g.*, to FIG. 4 and paragraphs 12 and 24-31 of the present application, a digitizer (42) is operable to receive a serial analog color signal (Analog Vout) having a predetermined sequence of color components wherein each color component represents an entire row of pixels (of a single color) across the source image (12). The digitizer (42) has a plurality of channels (51R, 51G, 51B) each operable to receive the serial analog color signal (Analog Vout) and to process a respective color component. It should be noted that the sensor (78) is distributed across the width of the source image (12), and each color light source (74R, 74G, 74B) is sequentially flashed once for each line of the source image (12). As a result, each color component in the serial analog color signal (Analog Vout) represents an entire row of pixels of a single color.

Kadowaki et al., on the other hand, does not disclose a digitizer operable to receive a serial analog color signal having a predetermined sequence of color components wherein each color component represents a row of pixels of a single color,

the digitizer having a plurality of channels each operable to receive the serial analog color signal and to process a respective color component. Kadowaki et al., at, *e.g.*, FIGS. 16(a) and 16(b), discloses an analog color signal processing circuit (44) that receives an analog color signal (SiG A) and produces a digital output signal (A DOUT). However, as shown clearly in FIG. 16(b), the analog color signal (SiG A) is simply a series of color bits (G1, B1, R1, etc.). The color components of the analog color signal (SiG A) do not represent a row of pixels of a single color in any way. This is reinforced by the fact that the digital output signal (A DOUT) is also a series of bits (G1, B1, R1, etc.). Therefore, claim 1 is not anticipated by Kadowaki et al.

Claims 13, 19 and 21-23

Claims 13, 19 and 21-23, as amended, are patentable for reasons similar to those recited above in support of the patentability of claim 1.

Claim 10

Claim 10, as amended, recites a digitizer operable to receive a serial analog color signal having a predetermined sequence of color components, the digitizer having a plurality of signal modification channels, one of the channels operable to sequentially modify each of the color components according to a corresponding modification parameter. Claim 10 also recites a controller coupled to the digitizer and operable to sequentially update the modification parameter to correspond to the color component that the one channel is modifying.

For example, referring, *e.g.*, to FIG. 4 and paragraph 32 of the present application, the digitizer (42) is operable to use only one of the channels (*e.g.*, 51R) to process all the color components of the serial analog signal (Analog Vout). The values stored in the register (*e.g.*, 56R) of the one channel are changed by the controller (80) to the modification parameters for the color component being processed.

Kadowaki et al., on the other hand, does not disclose a digitizer having a plurality of signal modification channels, one of the channels operable to sequentially modify each of the color components according to a corresponding modification parameter.

Kadowaki et al. also does not disclose a controller coupled to the digitizer and operable to sequentially update the modification parameter to correspond to the color component that the one channel is modifying. As discussed above, Kadowaki et al., at, *e.g.*, FIGS. 16(a) and 16(b), discloses an analog color signal processing circuit (44) that receives an analog color signal (SiG A). However, as shown clearly in FIG. 16(a), the analog color signal (SiG A) must be passed through a sample hold circuit (S/H 250) to produce color-separated signals (538-540). As a result, all three channels must be used in order to modify each of the color-separated signals (538-540). Therefore, claim 10 is not anticipated by Kadowaki et al.

Claims 18 and 20

Claims 18 and 20, as amended, are patentable for reasons similar to those recited above in support of the patentability of claim 10.

Claims 2-8, 11-12, 14-17 and 24

Claims 2-8, 11-12, 14-17 and 24 are patentable by virtue of their respective dependencies from independent claims 1, 10, 13 and 23.

Rejection of claim 9 under §103(a) as being unpatentable over Kadowaki et al.

Claim 9 is patentable by virtue of its dependency from independent claim 1.

CONCLUSION

In light of the foregoing remarks, claims 1-24 are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner contact the Applicants' attorney, Bryan Santarelli, at (425) 455-5575.

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Respectfully submitted,

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